



International Journal of Innovative Research in Science Engineering and Technology (IJIRSET)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)



Impact Factor: 8.699

Volume 14, Issue 6, June 2025

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www.ijirset.com |A Monthly, Peer Reviewed & Refereed Journal| e-ISSN: 2319-8753| p-ISSN: 2347-6710|

Volume 14, Issue 6, June 2025

|DOI: 10.15680/IJIRSET.2025.1406036|

A Novel Design of Area Efficient Full Adder Architecture using Reversible Logic Gates

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ABSTRACT: The design of reversible full adders in recent years has attracted a significant amount of attention because of the applications that they have in developing disciplines such as quantum computing, low-power computing, reversible logicbased computer systems. Reversible logic gates are the backbone of such systems because they use zero energy when their inputs and outputs are perfectly correlated. The conventional combinational logic circuits face problems like information loss energy inefficiency, which reversible computing addresses by storing input bits in the output, thereby improving efficiency. The efficiency of the processor is highly dependent on adders as they are basic to arithmetic and logic units. Using reversible gates like the Peres, Toffoli and Feynman gates, we design and implement a full adder. We propose an energy-tolerant, low-power reversible full adder that optimizes energy usage, decreases ancilla, minimizes garbage outputs, and reduces quantum cost through the use of reversibility design concepts.

KEYWORDS: Wallace Tree, VLSI architecture, Low Power, Analog to digital Converter, High speed applications.

I. INTRODUCTION

The rapid advancement of VLSI technology has led to increasing demand for low-power, high-performance, and areaefficient digital circuits. In traditional computing, logic operations are irreversible, leading to information loss and consequent heat dissipation as per Landauer's principle. This has become a significant concern in modern low-power circuit design. Reversible logic has emerged as a promising solution to this problem, as it allows the reconstruction of input vectors from output vectors, minimizing energy dissipation.

Reversible logic circuits have a one-to-one mapping between input and output states, ensuring that no formation is lost during computation.

These circuits are not only beneficial for low-power applications but are also essential in quantum computing, optical computing, and nanotechnology, where reversibility is a fundamental requirement. A critical component of arithmetic logic units (ALUs) and digital systems is the full adder, which performs binary addition of three input bits. Designing a full adder using reversible logic gates is crucial for building larger, more complex reversible arithmetic circuits. Among various reversible gates, the Peres gate is notable for its ability to implement logic functions with fewer gates and garbage outputs, leading to reduced circuit complexity. This project presents an area-efficient reversible full adder architecture that leverages reversible logic gates—specifically the Peres gate—to minimize circuit complexity, garbage outputs, constant inputs, and quantum cost. he proposed architecture aims to provide a compact and energy-efficient solution for arithmetic computation, which is essential in the design of advanced low-power systems such as quantum computers, optical computing, and DNA computing. Implemented using Xilinx Vivado 2016.2, this design offers practical insights into the realization of reversible logic in modern digital hardware platforms.



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II. MOTIVATION

The motivation for this project, "A Novel Design of AreaEfficient Full Adder Architecture using Reversible Logic Gates," comes from the growing need for low-power and efficient computing devices. Traditional circuits waste energy because they lose information during processing, which increases power consumption. Reversible logic helps solve this problem by preserving information, reducing energy loss, and making it useful for advanced technologies like quantum computing, low power chips, and nanotechnology.

III. RELATED WORKS

1.One of the key advancements in reversible logic design is the development of Peres gates, which have been widely utilized in full adder architectures. These gates are valued for their ability to perform XOR and AND operations simultaneously, making them highly efficient for generating carry-out signals in reversible full adders. Studies, such as those by Thapliyal et al. in 2005, demonstrated that Peres gate-based full adders could significantly reduce garbage outputs, leading to more compact and efficient designs.

2.Similarly, the Toffoli gate, another important reversible gate, has been extensively employed in arithmetic circuits due to its ability to implement universal logic operations. Research by Maslov et al.in 2003 highlighted its effectiveness in reducing the overall quantum cost of reversible circuits.

3. The Fredkin gate, known for its conditional switching capabilities, has been particularly useful for routing signals in reversible circuits. Its use in reversible full adders ensures efficient signal flow without the need for additional ancillary inputs, thereby reducing hardware complexity.

4. These gates have been instrumental in addressing the challenges of area efficiency in reversible logic design. Studies focusing on hybrid approaches, such as those by Islam et al. in 2009, combined these gates to minimize both garbage outputs and ancillary inputs, achieving significant improvements in circuit performance.

IV. SOFTWARE COMPONENT

Xilinx Vivado is the most complete design suite for synthesizing and analysing HDLs, including VHDL and Verilog, and is primarily used to design digital circuits for Xilinx FPGAs. Design entry is either through graphical interfaces or HDL coding, synthesis optimizes your design for performance and area, and implementation places and routes the design onto the FPGA architecture. Vivado also offers simulation tools to check functionality prior to deployment, as well as programming and debugging facilities such as the Integrated Logic Analyzer (ILA) to debug in real time. The IP Integrator lets users add prebuilt Intellectual Property (IP) cores into their designs, accelerating development. Also, Vivado supports a large number of Xilinx devices and comes with version control features for collaboration among teams.

V. PROPOSED MODEL

The major purpose of the recommended research is to formulate the minimal energy, less optimal speed and minimal complexity Wallace tree encoder that is used in both the traditional and modern conversion procedure. In the recommended design energy consumption of the Wallace tree encoder that is diminished by the corrected design of the complete adder. The adapted complete adder comprises of about transistors. By reducing the number of the transistors, the energy consumption of the complete adder can be reduced. Fig indicates a more modified full adder. Fig. Modified hybrid full adder used in Wallace Tree encoder Module consists of five transistors. Transistors form XNOR gate and forms the inverter. Hence the circuit complexity is reduced by using 3T XNOR through PTL. The second module M2 with 4 transistors forms XNOR gate. It produces the sum output of full adder. The carry output of the full adder is generated by module which is realized by four transistors. For the propagation of the carry, only one transmission gate is used in the proposed design. It reduces the propagation delay.



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VI. RESULTS AND DISCUSSIONS

The area-efficient full adder was implemented using Peres gates and simulated on Xilinx Vivado 2016.2. The design was verified for all input combinations and produced correct sum and carry outputs, confirming functional accuracy. Synthesis results showed a significant reduction in gate count compared to conventional designs. The number of garbage outputs and constant inputs was minimized, contributing to a more compact and efficient circuit. The use of Peres gates led to a lower quantum cost, making the design suitable for both low-power VLSI and quantum computing applications. The circuit also consumed less area and exhibited improved hardware resource utilization. Compared to previously published reversible full adder models, this design offers better optimization in terms of power, area, and performance. Overall, the results demonstrate that the proposed reversible full adder architecture is both functionally reliable and resource-efficient, supporting its potential use in future energy-efficient digital systems.





VII. CONCLUSION

In conclusion, the project proposes an enhanced low-power reversible full adder tailored for energy-efficient applications. It offers a comprehensive examination of reversible circuits featuring energy-efficient full adders, contrasting them with conventional CMOS circuits. The primary objective of reversible logic designs is to minimize ancillae inputs and garbage outputs. The proposed methodology reduces garbage outputs by 75% and reduces the required number of transistors for the design by 50%, compared to existing literature.



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JDOI: 10.15680/IJIRSET.2025.1406036S.noParameteTraditional
Full AdderProposed
Reversible
Exult

| | | Full Adder | Reversible Full Adder |
|---|---------------------|------------|-----------------------------|
| 1 | Transistor Count | 44 | 18 |
| 2 | Garbage Output | 1 | 0 |
| 3 | Power | 1.5W | 0.978W |

REFERENCES

- 1. R K Ahirwar, SS Gawande," Reversible Arithmetic Logic Unit Based on Bidirectional Gate", Electronics and Communication Engineering, Vol.2 ,2025.
- 2. S Dasgupta, S Pandey, D Roy, A Maity, Antarik Sinha, Mihir Lal Saha," Design and Implementation of an Efficient Quantum Cost Optimized Adder using Reversible logic gates",2025.
- 3. Swetha Siliveri, N Siva Sankara Reddy, "Design and Optimization of Reversible Arithmetic Unit Using Modified Gate Diffusion Input Logic", Volume 112,2025.
- Kanchan S Tiwari, Revati M Wahul, Sagar D Shinde, Manisha A Dudhedia Varsha P Gaidwad Pranav," Design and Implementation of Low Power Generic Reversible Binary Coded Decimal Adder on Artix-7 FPGA", Vol 12, Issue 2, p730,2025.
- 5. Ravindra Kumar Ahirwar, Suresh S Gawande, "VHDL Implementation of Reversible Arithmetic
- 6. Logic Unit using Bidirectional Gate", Vol 2 No.1(2025).
- 7. D Rohini, M Harsha Vardhan Reddy , G Kishor, "Power Optimized Carry Select Adder Using Reversible Logic Gates ",2025.
- 8. B. Naresh Kumar Reddy, and Subrat Kar, "Performance Evaluation of Modified Mesh-based NoC architecture," Computers and Electrical Engineering, Vol. 104, 2024.
- 9. Sai Kumar and B. Naresh Kumar Reddy, "An Efficient Real-Time Embedded Application Mapping for NoC Based Multiprocessor System on Chip," Wireless Personal Communications, Vol. 128, 2024. [9]
- 10. Raghava Rao, K., Naresh Kumar Reddy, B. & Kumar, A.S. "Using advanced distributed energy efficient clustering increasing the network lifetime in wireless sensor networks", Soft Computing, Vol. 27, pp. 15269-15280, 2023.
- A. S. Kumar, M. Deekshana, V. B. Sreenivasulu, N. A. Kumari and G. Shanthi," Device Analysis of Vertically Stacked GAA Nanosheet FET at Advanced Technology Node," 2023 3rd International Conference on Advances in Computing, Communication, Embedded and Secure Systems (ACCESS), India, pp. 274-279, 2023.
- S. Kumar, K. N. Rao, A. Sujith, T. Dhanuja and M. V. S. Vinay, "Design and Implementation of 1KB SRAM array in 45 nm Technology for Low-Power Applications," 2023 3rd International Conference on Advances in Computing, Communication, Embedded and Secure Systems (ACCESS), India, pp. 245-250, 2023.
- 13. Aruru Sai Kumar et al., "Nanosheet Field Effect Transistor Device and Circuit Aspects for Future Technology Nodes," ECS Journal of Solid-State Science and Technology, Vol. 12, No. 8, 2023.
- 14. Suparshya babu sukhavasi, Thanu Sri Gandham, Susrutha babu sukhavasi, Meuva veera Venkata bhargav.,"Realization of low power and efficient sequential circuits using reversible logic gates,vol.2.2025









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